REMARKS

Counsel for Assignee has received and reviewed the first Office Action in this case. In that Action claims 11-26 were presented for examination and were rejected under 35 U.S.C. § 102 and 103. The Examiner has cited various references against the claims. By this response counsel has amended the claims to highlight key features of Applicants' invention not shown or suggested by the cited references.

Brief Discussion of Applicants' Invention

Applicants' invention here involves a new technique for designing integrated circuits in a more optimal manner. Conventional design tools for performing such activities suffer from a number of disadvantages, notably difficulties with assuring uniform timing of the completed integrated circuit. In the prior art, as described in the specification and typified by the cited references, the design tools partition the circuit to be designed into relatively low level constituent parts. These parts are then designed automatically and combined with each other to create a circuit having the desired functionality. The automated nature of the process means that the resulting circuit or system is sometimes inefficient in terms of power, timing, integrated circuit area consumption, etc.

Furthermore, the tools conventionally used for designing circuits often use automatic routing technology to place the signal lines which must interconnect all of the elements of the integrated circuit to each other. The automatic nature of the routing has several undesirable results, for example, resulting in unexpectedly long signal paths which require increased power, or creating timing difficulties. In summary, the techniques of the prior art create functional circuits; however, circuits which are far from optimal in terms of desired goals such as timing, performance, area consumption, etc.

The techniques described in Applicants' specification disclose an approach for designing integrated circuits which results in much higher performance circuits which are more easily designed. Using the approach developed by the inventor, large sections

of the circuit, referred to as a "group" are designed and optimized to provide generic functionality which can be reused in other circuits. For example, a group might provide a complex circuit element such as an arithmetic logic unit.

Importantly, the physical layout for a group will have a predetermined boundary with predetermined interconnection points on the boundary and/or across the circuit itself. Most importantly, however, all of the interconnections among the elements within a group are made on fewer than all of the potential interconnection layers available using that particular integrated circuit technology. For example, if the integrated circuit is to be manufactured using four-layer metal process technology, fewer than four layers will be used to interconnect the elements of a group. This feature, described in Applicants' specification and claimed in each of the independent claims, allows the performance of a group to be "fixed." The performance is fixed in the sense that once the group is designed and laid out, no further connections are provided within the group, hereby assuring required performance and density will not be changed for that group by later design additions. Instead, only additional connections are provided to enable connecting the group to other groups or to I/O pins of the integrated circuit itself. By designing the circuit in this manner, the performance of the group is fixed and assured to meet the desired specification.

When the groups are interconnected, routing of interconnection layers is only necessary among, not within, groups. These interconnections are provided on layers other than the layers used to interconnect within a group. The result is overall increased circuit performance.

In independent claim 11, this limitation is specified by claim language which calls for intra-group interconnections to be defined in certain layers, and inter-group connections to be provided only on other layers, i.e., layers not used for intra-group connections. This allows timing and performance to remain assured once the group itself is completely designed. Independent claim 14 includes similar limitations, but is phrased differently.

The Prior Art

The Examiner has rejected claims 11-13 under *Andreev, et al.*, U.S. Patent 6,182,272. *Andreev, et al.*, does teach a method for routing connections in a layer. It does not appear to describe groups of on the order of 300-5000 gates, and more importantly does not disclose the particular routing technique claimed in Applicants' claims as now presented for examination. While it is not explicitly stated, the routing technique of *Andreev* is one in which a gate array is routed, involving myriads of connections among myriads of cells. See, e.g., column 5 at lines 33-49, suggesting the routing performed is among cells, rather than among larger blocks of circuitry - such as groups - as described by Applicant.

Claims 14-18 were rejected based upon *Zhen*, U.S. Patent 6,298,468, in view of *Dangelo, et al.*, U.S. Patent 5,880,971. The *Zhen* patent focuses primarily upon pin location optimization, and in particular, in locating certain pins closer to certain components and further from other components, based upon the load imposed. See, e.g., column 3, lines 14-43. *Zhen* does not appear to teach the particular technique employed by Applicant of providing groups of circuits which are interconnected on fewer than all potential layers of interconnections, then using the remaining layers to interconnect among the groups. Nor does the other reference cited - *Dangelo, et al.*, '971 - appear to teach this feature of Applicants' invention. *Dangelo, et al.*, seems to focus on an automated layout technique in which the structural layout is derived from a behavioral description using steps similar to those described in the background of Applicants' specification, such as behavioral simulation using VHDL, partitioning, logic synthesis, physical simulation, etc. (See column 3, lines 9-65.) Because neither *Zhen* nor *Dangelo, et al.*, teach the important aspect claimed relating to Applicants' invention regarding the routing of wiring, counsel submits that taken separately or combined, the claims presented here are patentable over those references.

All of the remaining claims in this case examined by the Examiner are dependent claims. Because the independent claims patentably distinguish the cited

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references for the reasons discussed above, counsel believes that all claims now presented for examination patentably distinguish those cited references.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

A marked up copy of amended claims is provided in Appendix A. A clean copy of all pending claims are in Appendix B.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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APPENDIX A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claim 11 has been amended as follows:

11. (Amended) A method of determining a definition of a physical representation of at least a portion of an integrated circuit, the integrated circuit performing logic operations, arithmetic operations, control operations, and memory operations, the integrated circuit being comprised of a plurality of groups, the groups being largely comprised of between 300 and 5000 gates, the groups being present in a library of groups, **[with]**each group having a **[being]**predefined **[in terms of]**logical and physical layout**[s]**, and having a plurality of layers within which intra-group interconnections are provided among various elements within the group, the physical layout having predefined boundaries with predefined interconnection points**[along the physical boundaries]**, and at least some of the groups being amalgamated into functions, the functions being present in a library of functions, the method comprising:

when the intra-group interconnections are defined, providing all such interconnections on fewer than all of the plurality of layers;

selecting an item, the item being a group or a function, for placement on a layout;

placing the item on the layout;

selecting a further item for placement on the layout;

placing the further item on the layout; and

defining inter-group interconnections between the item and the further item, the inter-group interconnections being provided entirely on layers that are not used for the intra-group interconnections.

Claim 12 has been canceled without prejudice.

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Claims 13, 14 and 19-21 have been amended as follows:

13. (Amended) The method of claim 11 **[12]**wherein the plurality of layers are each layers having electrically conductive material thereon, with vias from at least one adjoining layer connected thereto**[separated by metallization having vias]**.

14. (Amended) An integrated circuit comprised of a plurality of regularly placed circuit groups, the circuit groups being on an order of magnitude of 1000 gates, the circuit groups having predefined connection points, each group having interconnections within that group on a plurality of layers of the integrated circuit, the plurality of layers being less than all of the layers, at least some of the circuit groups being amalgamated into sets of groups.

19. (Amended) The integrated circuit of claim 14 wherein **[the integrated circuit has a number of metal layers, with]**the plurality of circuit groups are provided to have electrical connections within them solely on a first plurality of electrically conductive **[metal]**layers, and wherein clock and power signals are provided on electrically conductive **[metal]**layers other than the first plurality of electrically conductive **[metal]**layers.

20. (Amended) The integrated circuit of claim 19 wherein the clock and power signals are on the same **[metal]**layer.

21. (Amended) The integrated circuit of claim 20 wherein global routing signals among the plurality of groups are transferred among the groups on at least one electrically conductive **[a metal]**layer other than the first plurality of electrically conductive **[metal]**layers or the **[metal]**layer used for **[of]**the clock and power signals.

APPENDIX B

CLEAN VERSION OF ALL PENDING CLAIMS

11. (Amended) A method of determining a definition of a physical representation of at least a portion of an integrated circuit, the integrated circuit performing logic operations, arithmetic operations, control operations, and memory operations, the integrated circuit being comprised of a plurality of groups, the groups being largely comprised of between 300 and 5000 gates, the groups being present in a library of groups, each group having a predefined logical and physical layout, and having a plurality of layers within which intra-group interconnections are provided among various elements within the group, the physical layout having predefined boundaries with predefined interconnection points, and at least some of the groups being amalgamated into functions, the functions being present in a library of functions, the method comprising:

when the intra-group interconnections are defined, providing all such interconnections on fewer than all of the plurality of layers;

selecting an item, the item being a group or a function, for placement on a layout;

placing the item on the layout;

selecting a further item for placement on the layout;

placing the further item on the layout; and

defining inter-group interconnections between the item and the further item, the inter-group interconnections being provided entirely on layers that are not used for the intra-group interconnections.

13. (Amended) The method of claim 11 wherein the plurality of layers are each layers having electrically conductive material thereon, with vias from at least one adjoining layer connected thereto.

14. (Amended) An integrated circuit comprised of a plurality of regularly placed circuit groups, the circuit groups being on an order of magnitude of 1000 gates, the circuit groups having predefined connection points, each group having interconnections within that group on a plurality of layers of the integrated circuit, the plurality of layers being less than all of the layers, at least some of the circuit groups being amalgamated into sets of groups.

15. The integrated circuit of claim 14 further comprising trailers attached to groups.

16. The integrated circuit of claim 15 wherein the trailers provide physical translation of interface signals associated with the predefined connection points.

17. The integrated circuit of claim 15 wherein the trailers provide for buffering of interface signals associated with the predefined connection points.

18. The integrated circuit of claim 15 wherein the trailers provide for staging of interface signals associated with the predefined connections points.

19. (Amended) The integrated circuit of claim 14 wherein the plurality of circuit groups are provided to have electrical connections within them solely on a first plurality of electrically conductive layers, and wherein clock and power signals are provided on electrically conductive layers other than the first plurality of electrically conductive layers.

20. (Amended) The integrated circuit of claim 19 wherein the clock and power signals are on the same layer.

21. (Amended) The integrated circuit of claim 20 wherein global routing signals among the plurality of groups are transferred among the groups on at least one electrically conductive layer other than the first plurality of electrically conductive layers or the layer used for the clock and power signals.

22. The integrated circuit of claim 21 wherein the global routing signals are on a plurality of metal layers.

23. The integrated circuit of claim 19 wherein the groups comprise data path groups and memory groups.

24. The integrated circuit of claim 23 wherein the groups further comprise control groups.

25. The integrated circuit of claim 24 wherein the groups further comprise I/O groups.

26. The integrated circuit of claim 25 wherein the groups further comprise analog groups.